

THE SINGLE-ENDED S-MATRIX

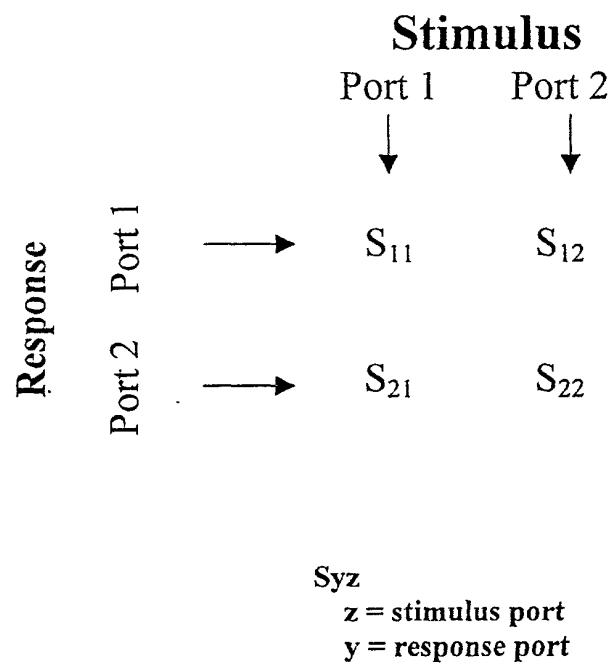


FIG. 1(a)

(Related Art)

THE MIXED-MODE S-MATRIX

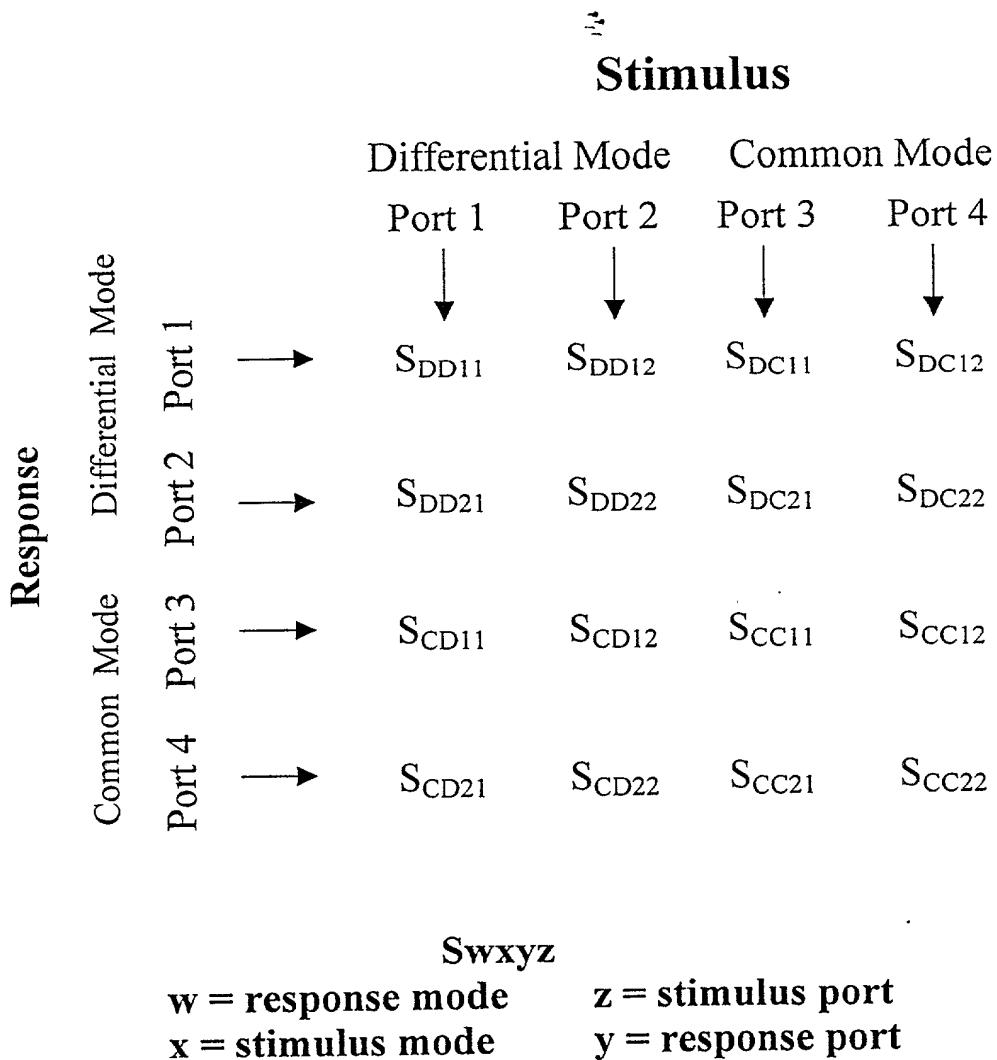


FIG. 1(b)
(Related Art)

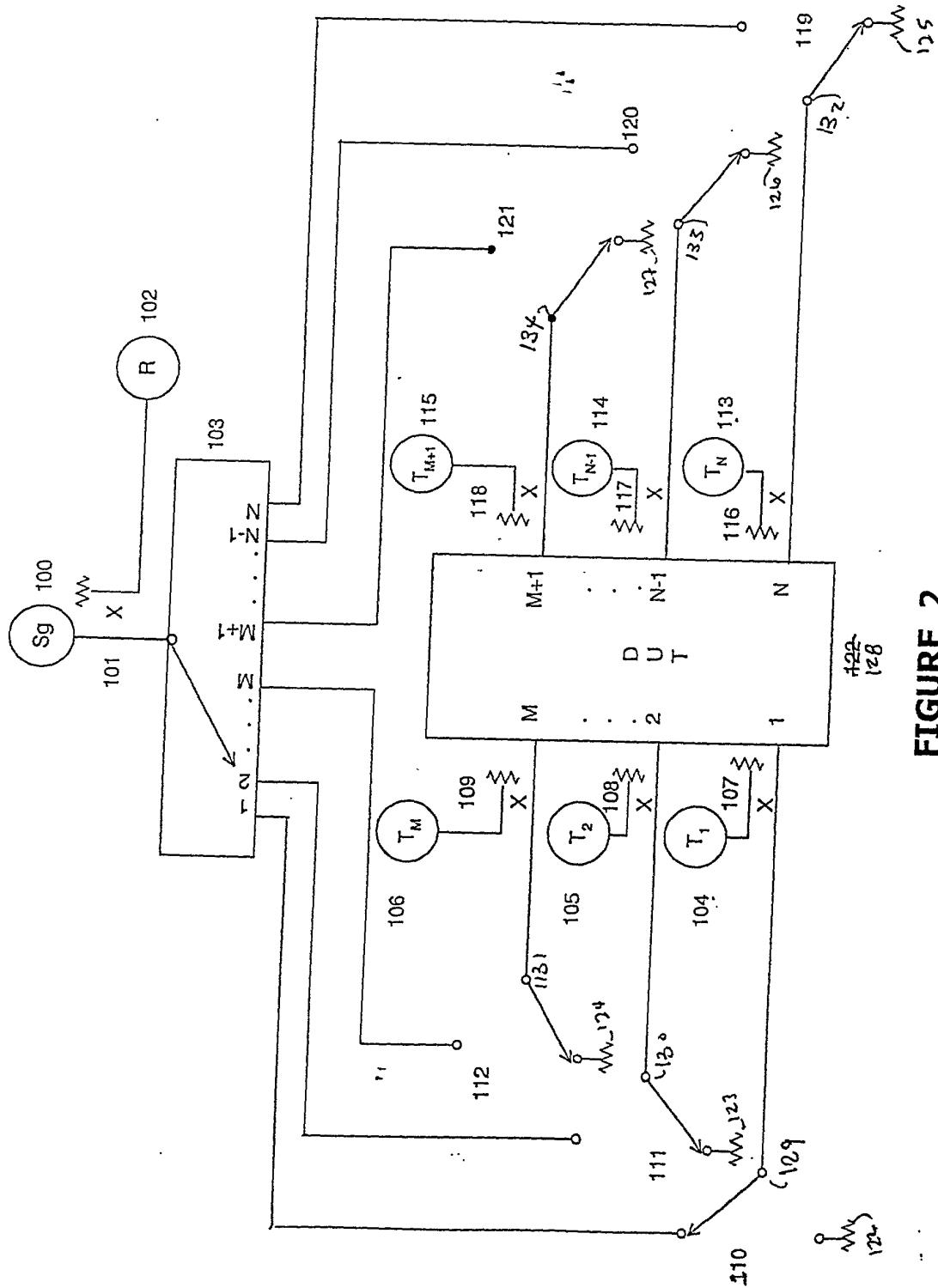


FIGURE 2

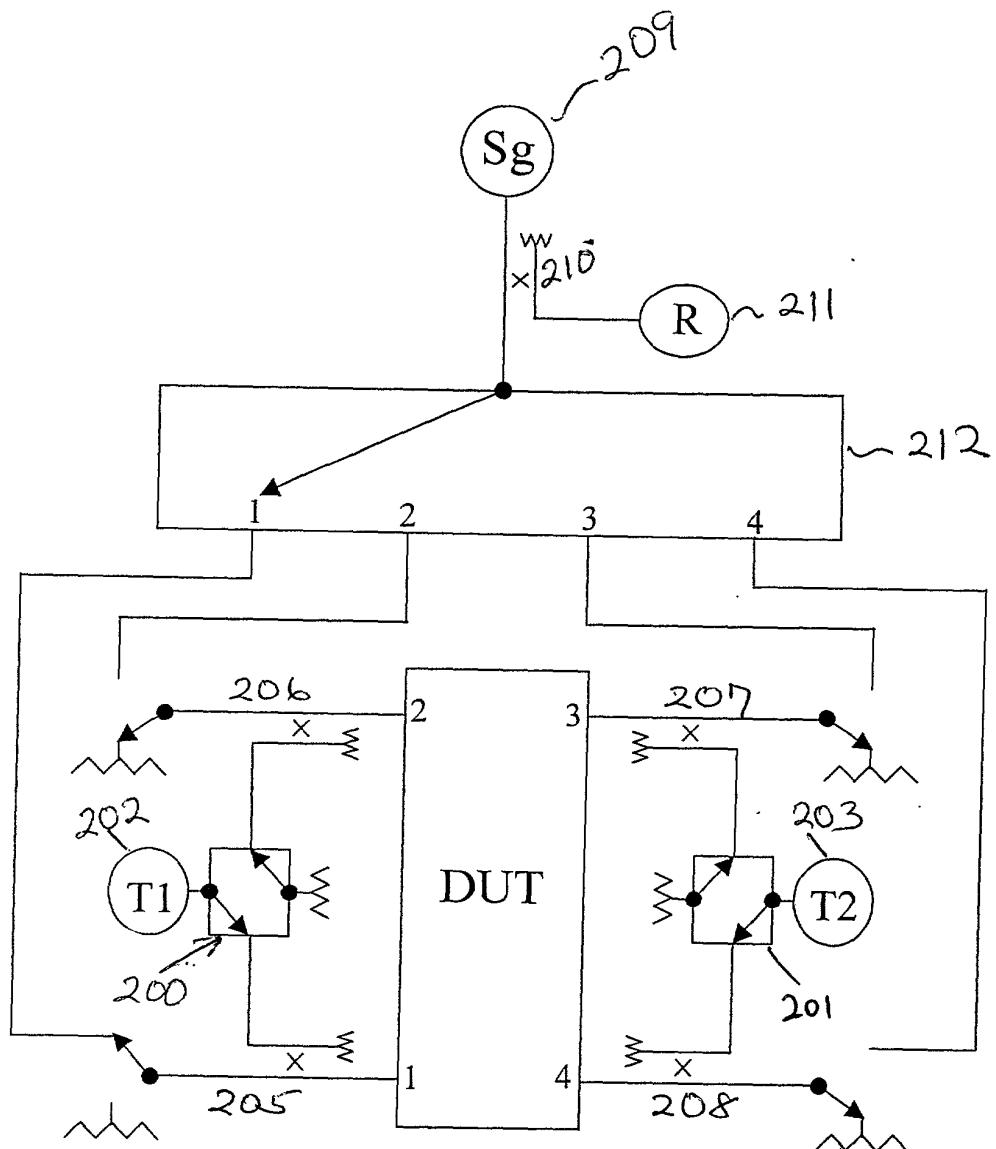


FIGURE 3

9-Port MTS Using 1 Reference & 3 Test Channel Receiver

20

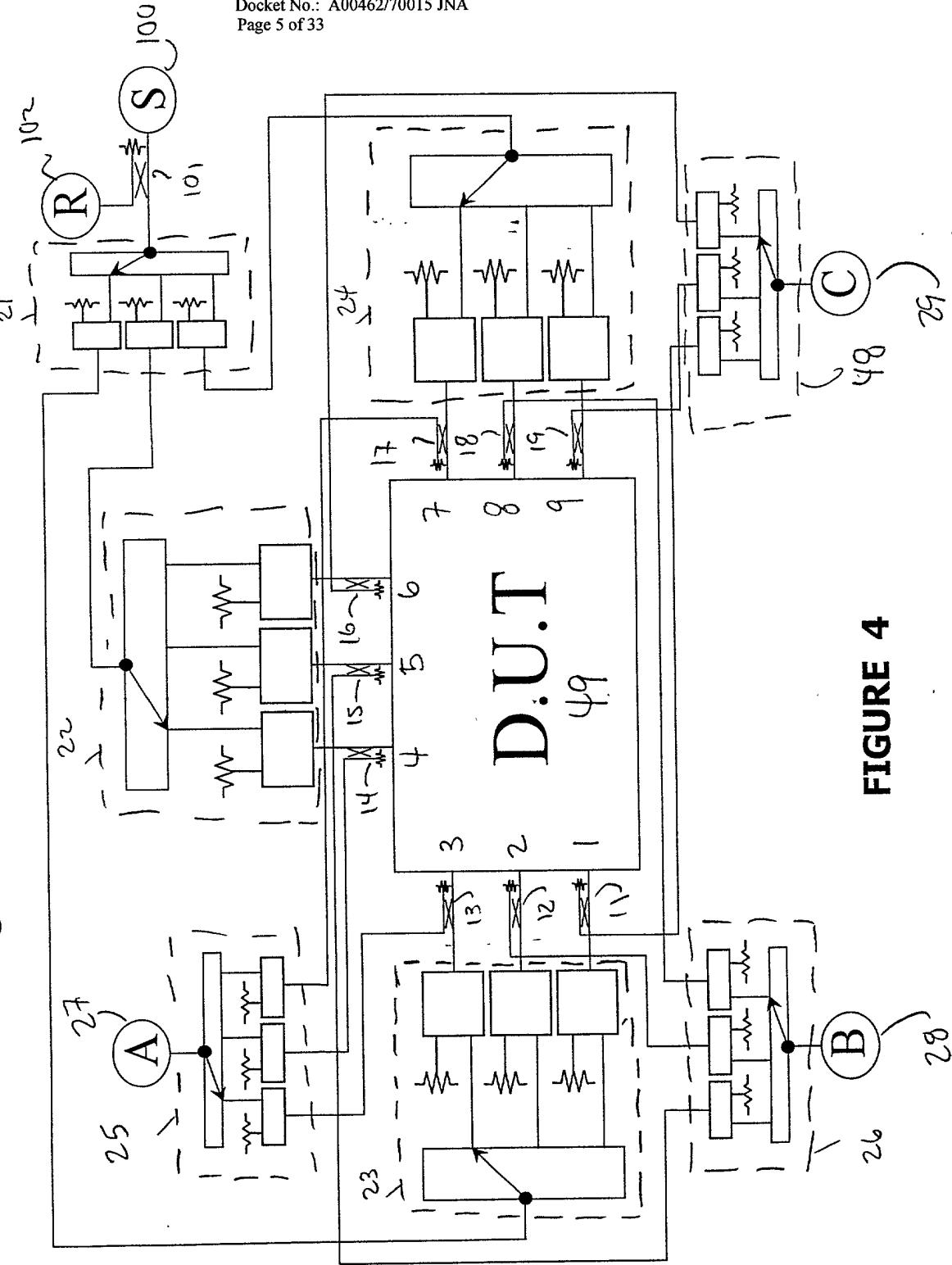


FIGURE 4

6-Port MTS Using 1 Reference & 2 Test Channel Receiver

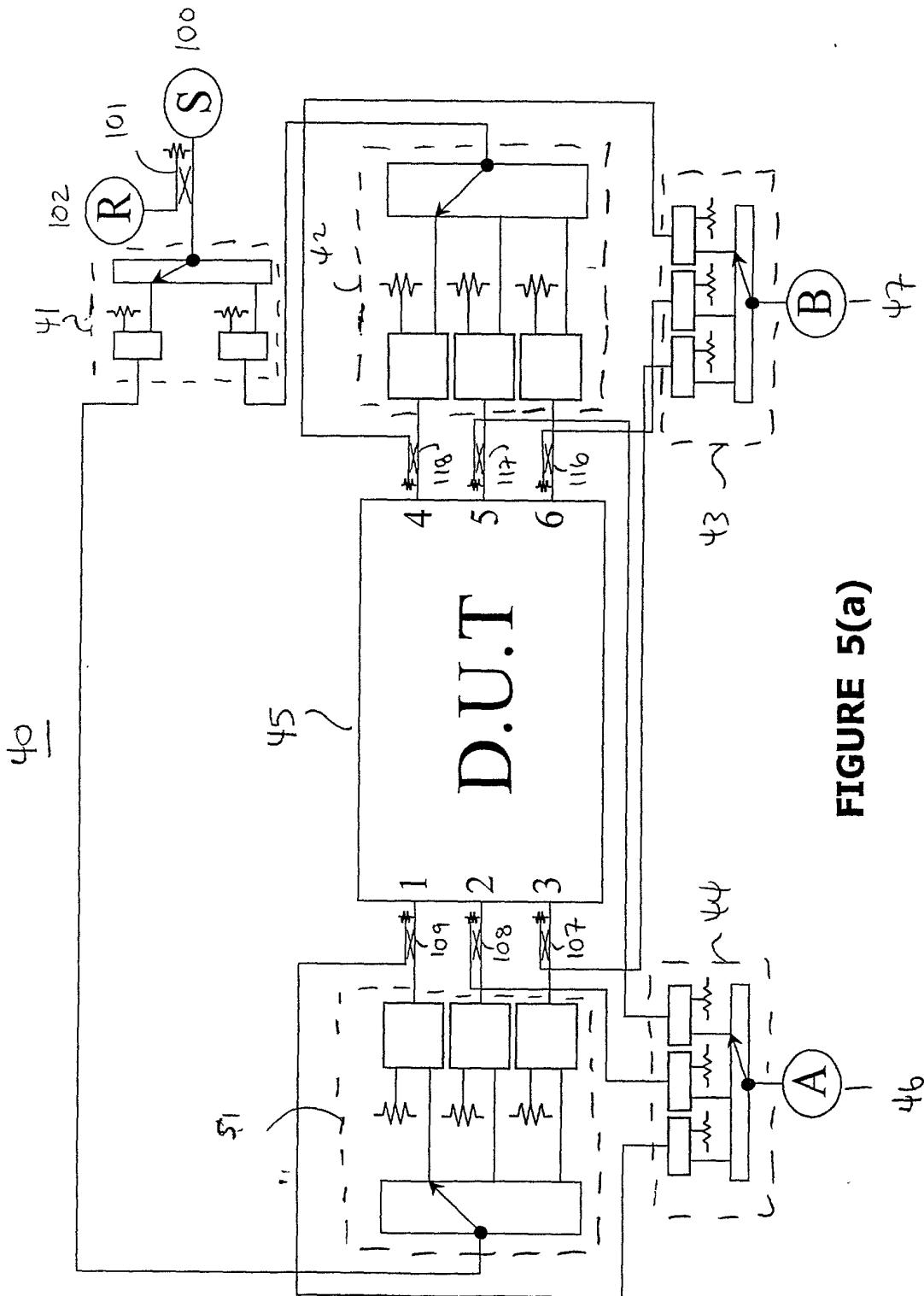


FIGURE 5(a)

6-Port MTS Using 1 Reference & 3 Test Channel Receiver

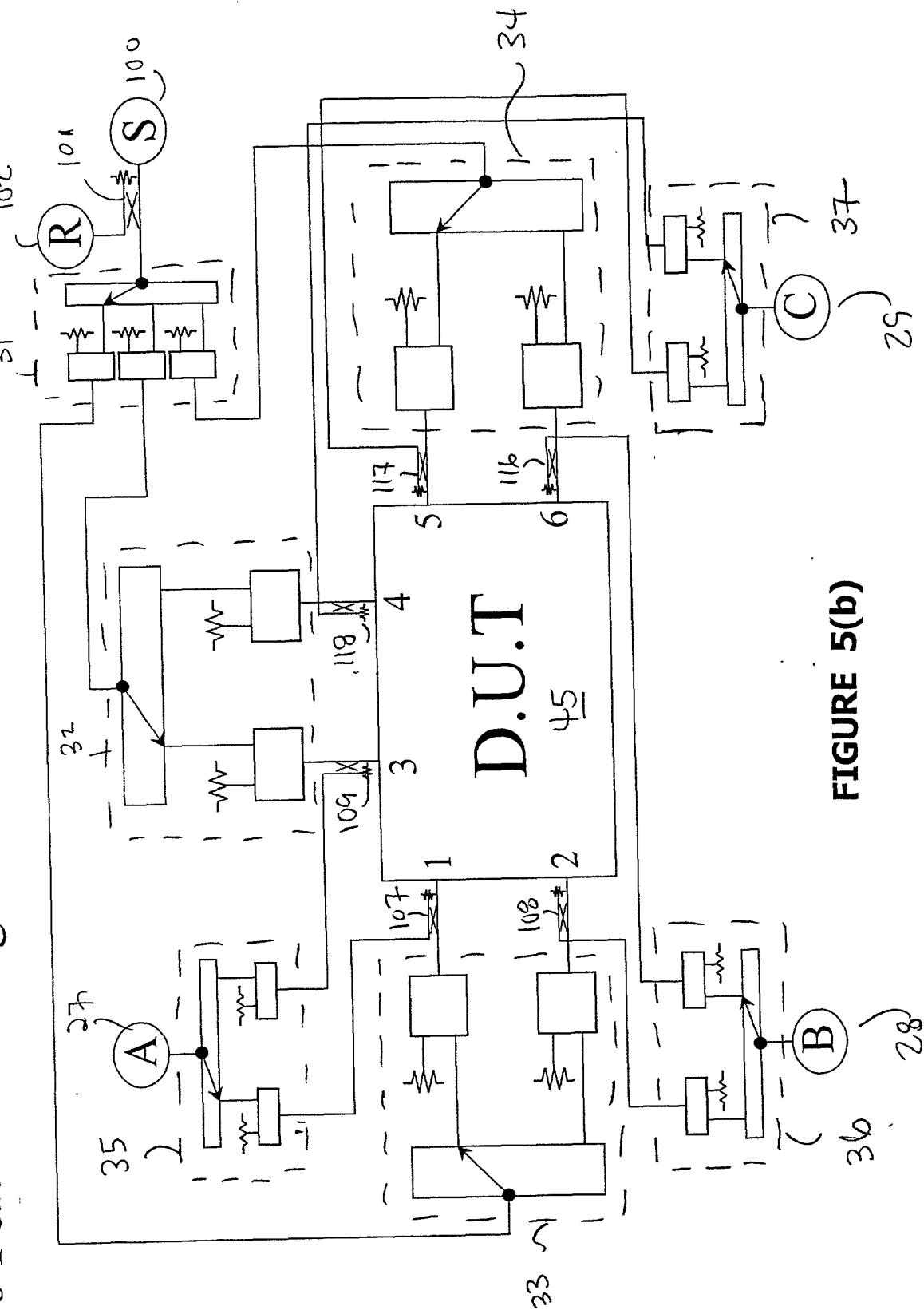


FIGURE 5(b)

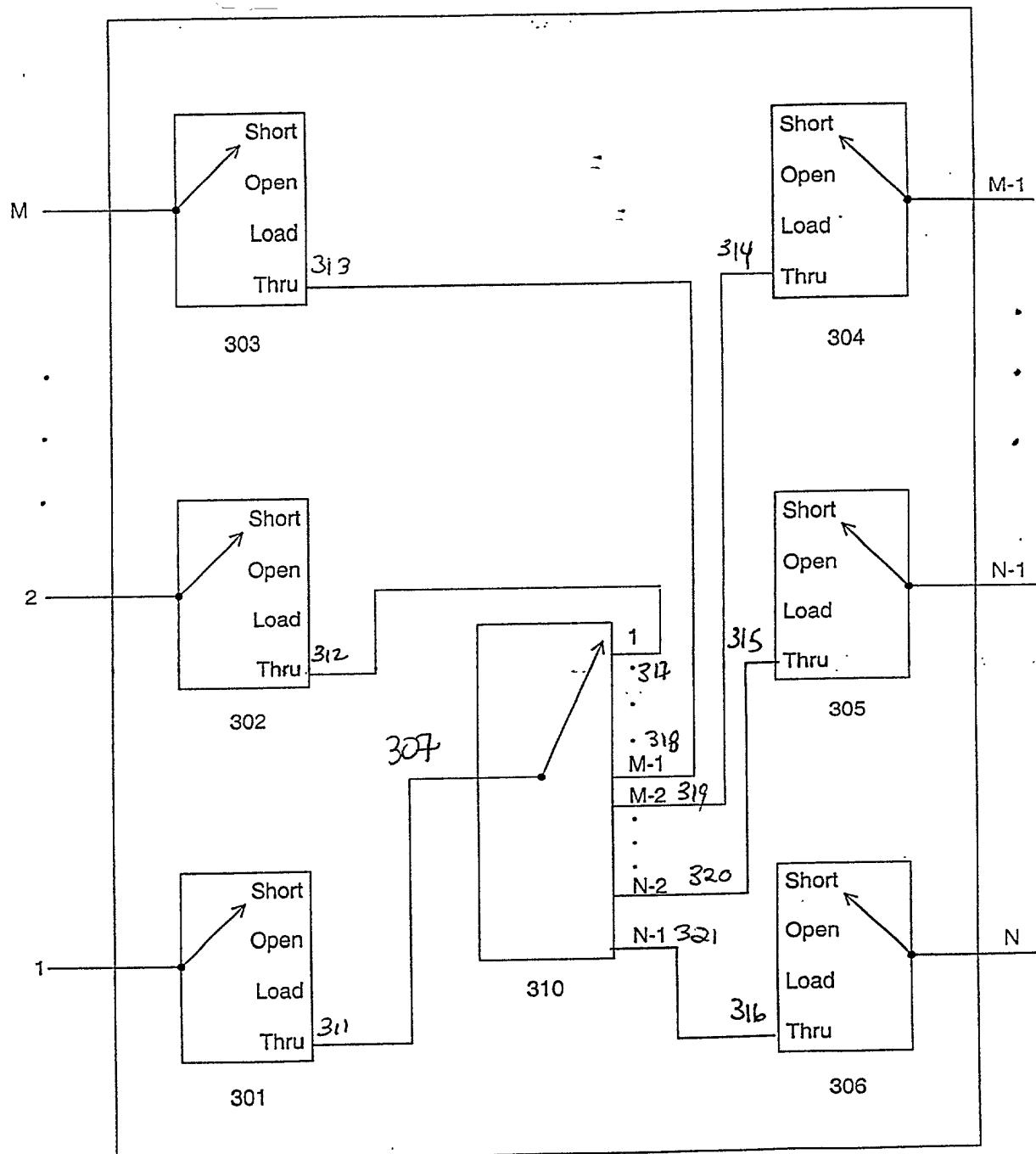


FIGURE 6
(Related Art)

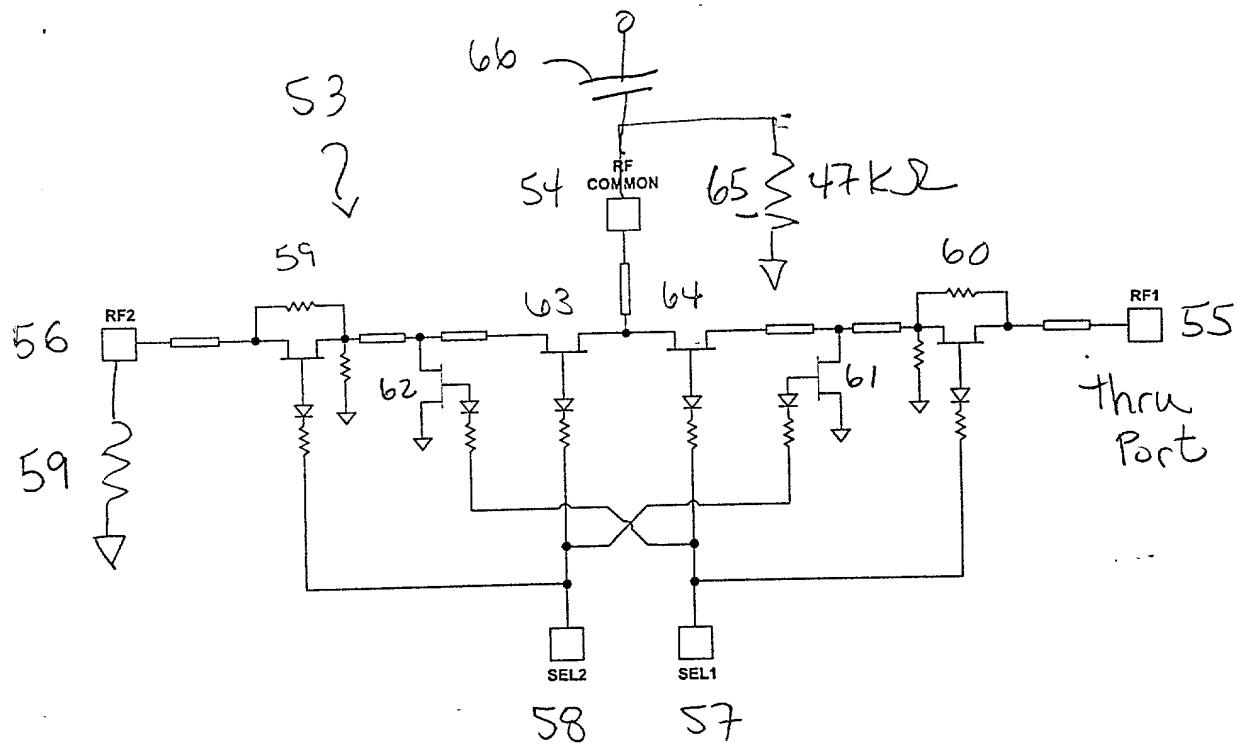


FIGURE 7

FET Switch Configurations

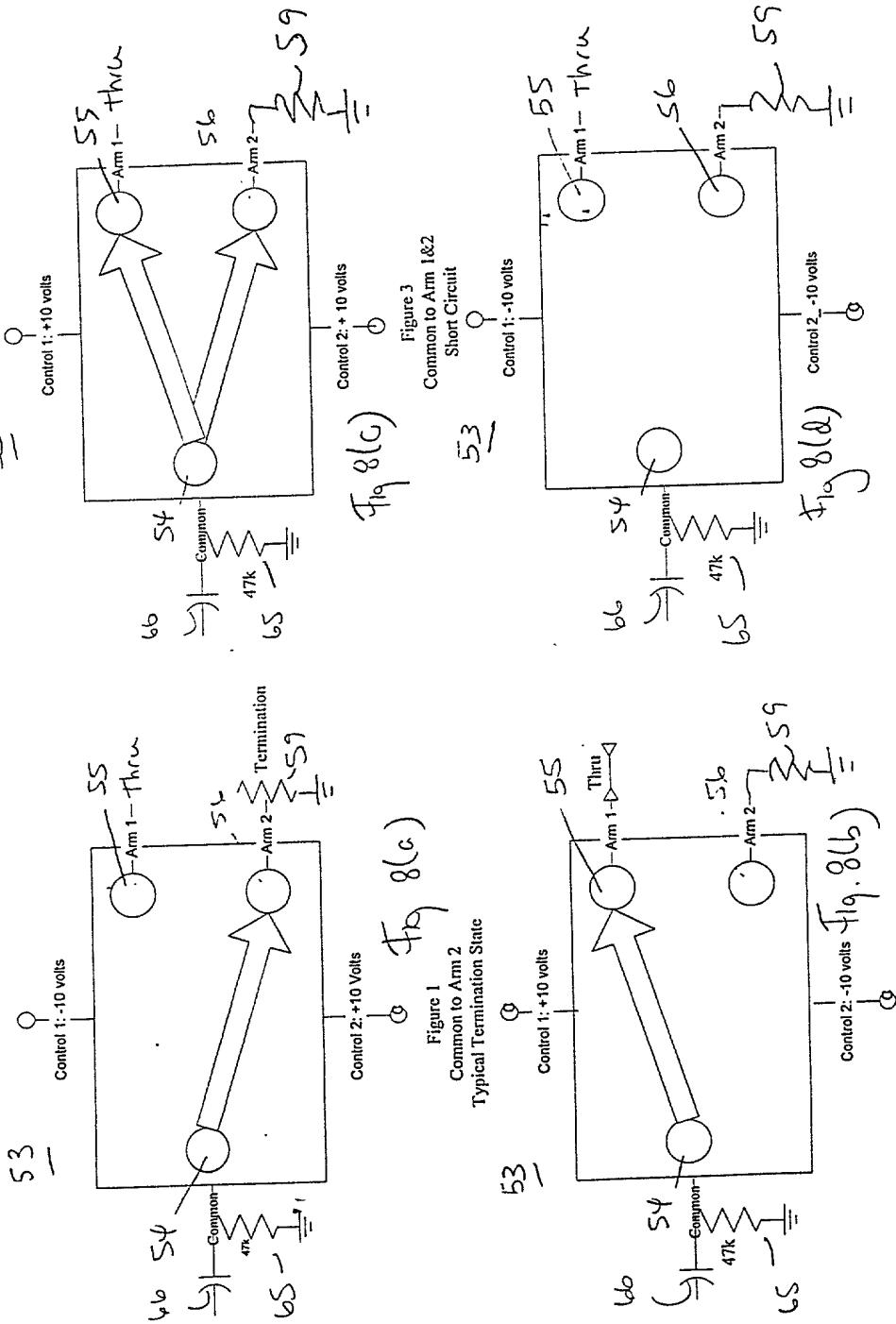


Figure 1
 Common to Arm 2
 Typical Termination State

Figure 4
 Both Arms of
 Open Circuit

FIGURE 8

Figure 2
 Common to Arm 1
 Thru condition

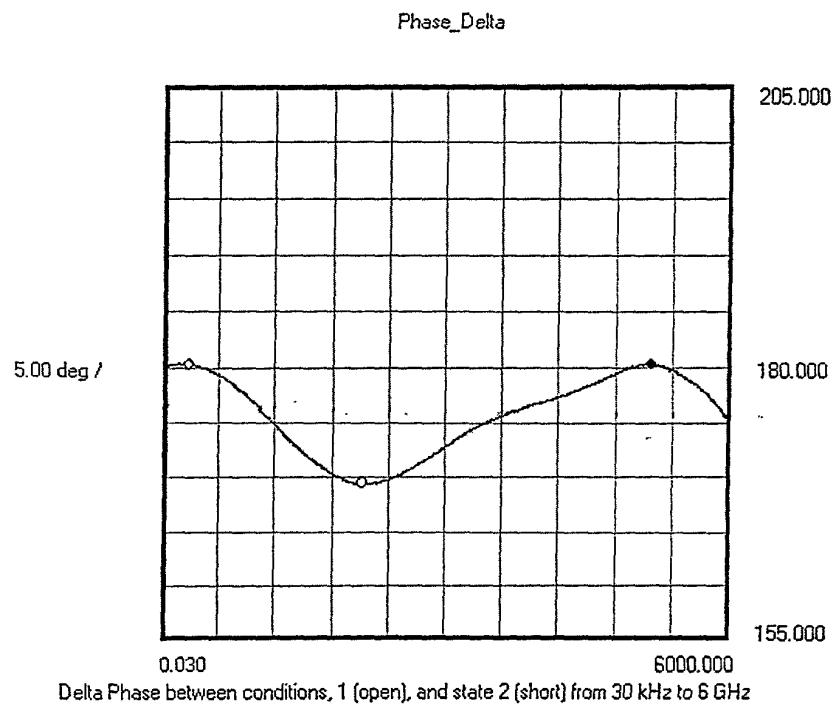


FIGURE 9

S22

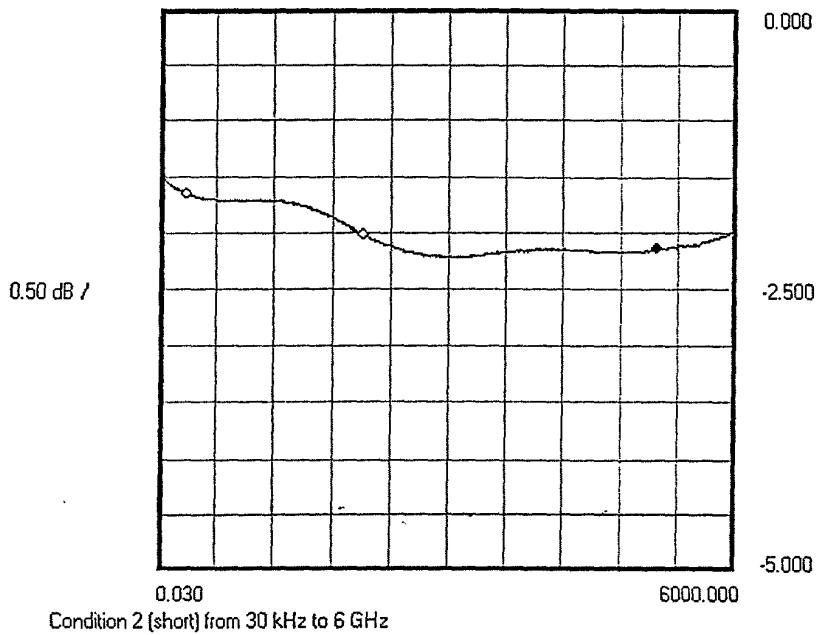


FIGURE 10

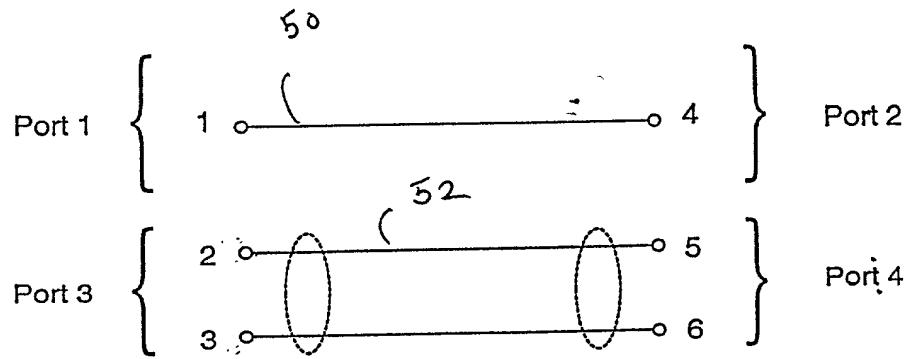


FIGURE 11

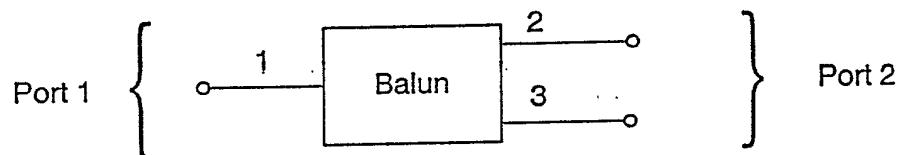


FIGURE 13

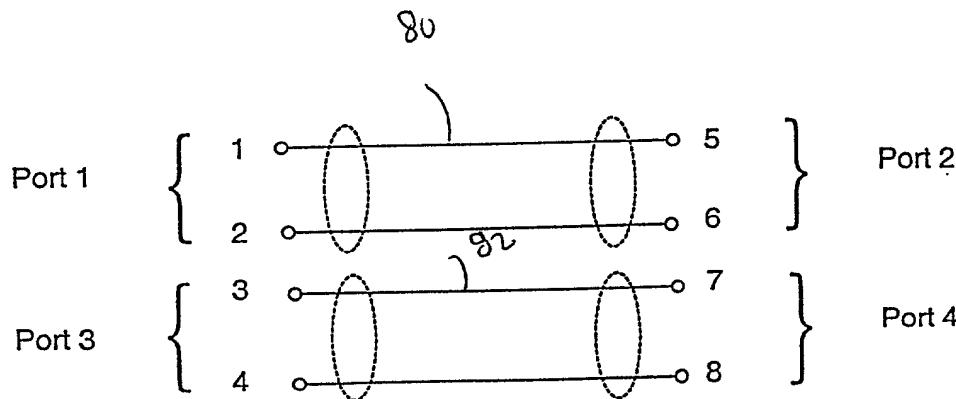


FIGURE 14

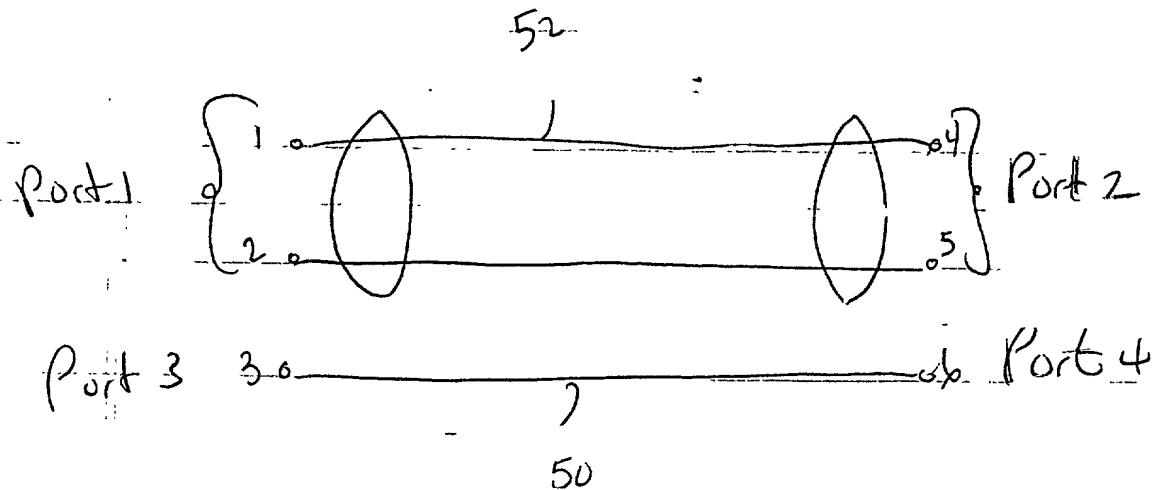


FIGURE 12

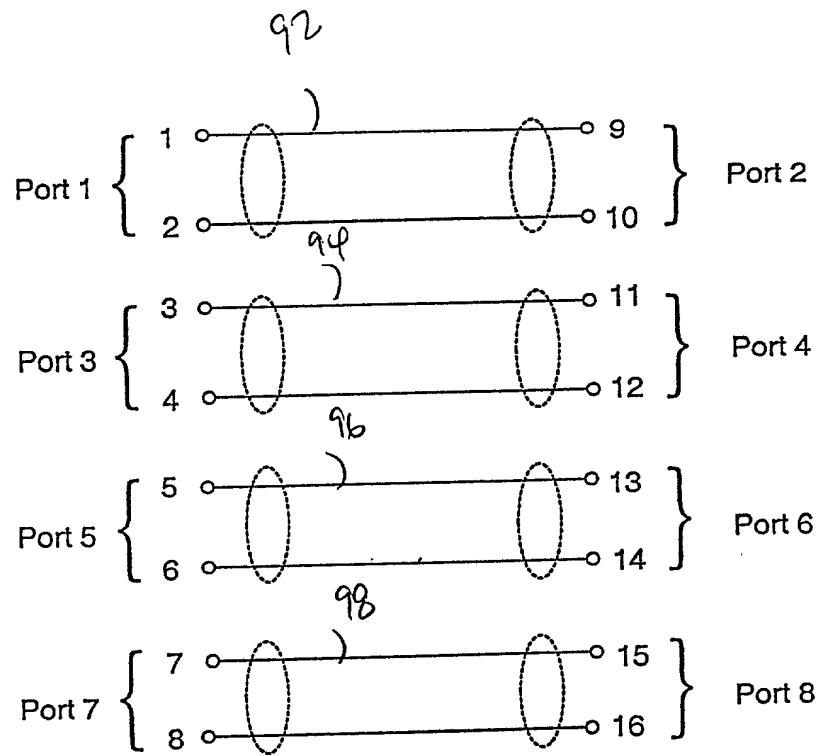


FIGURE 15

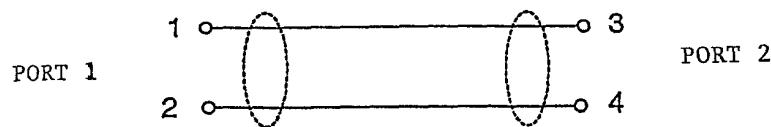


FIGURE 16

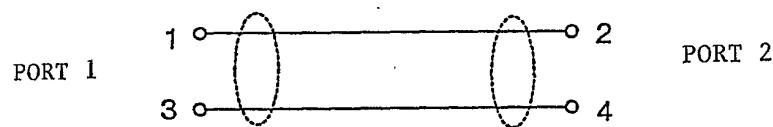


FIGURE 17

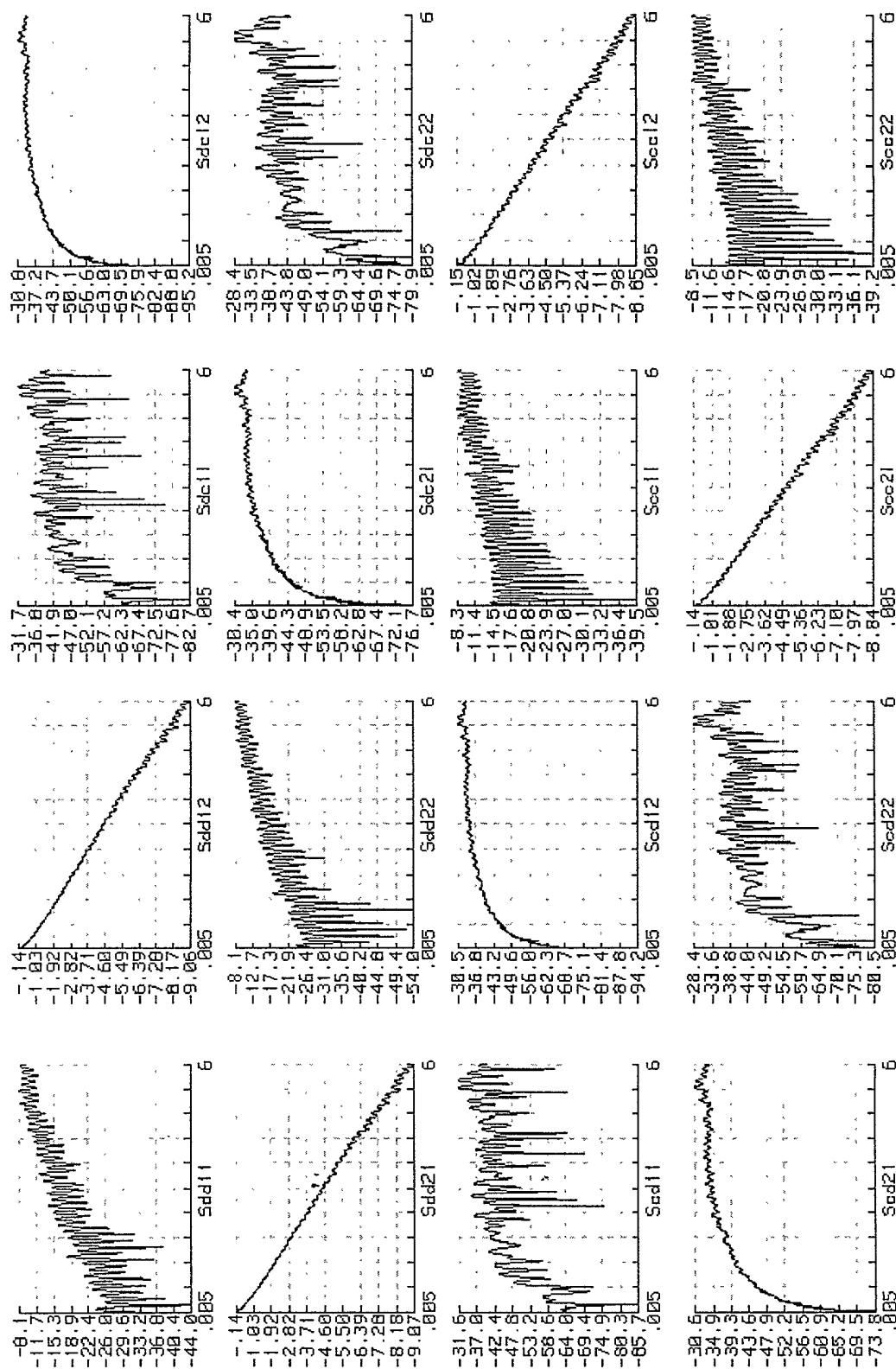


FIGURE 18

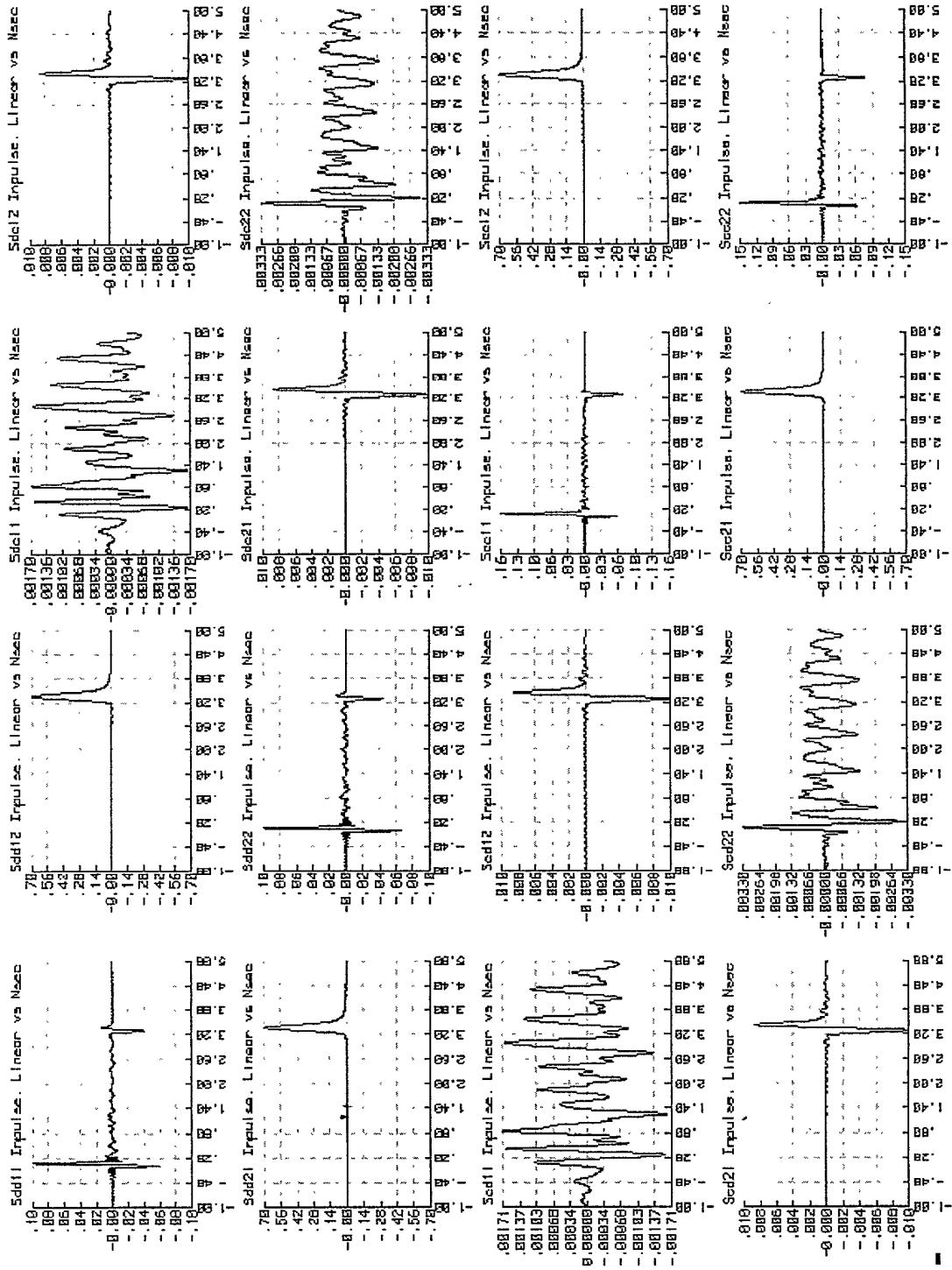
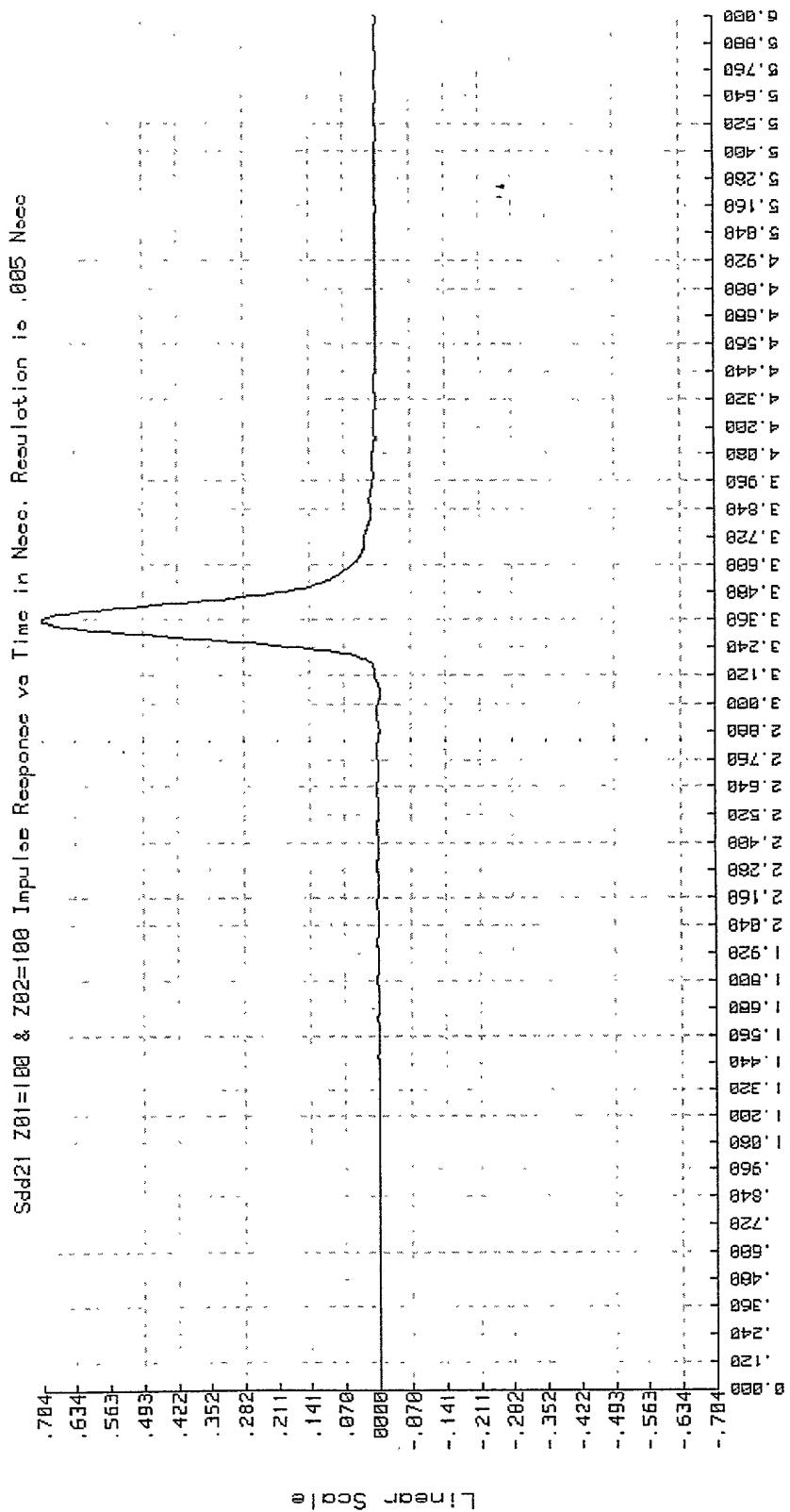


FIGURE 19



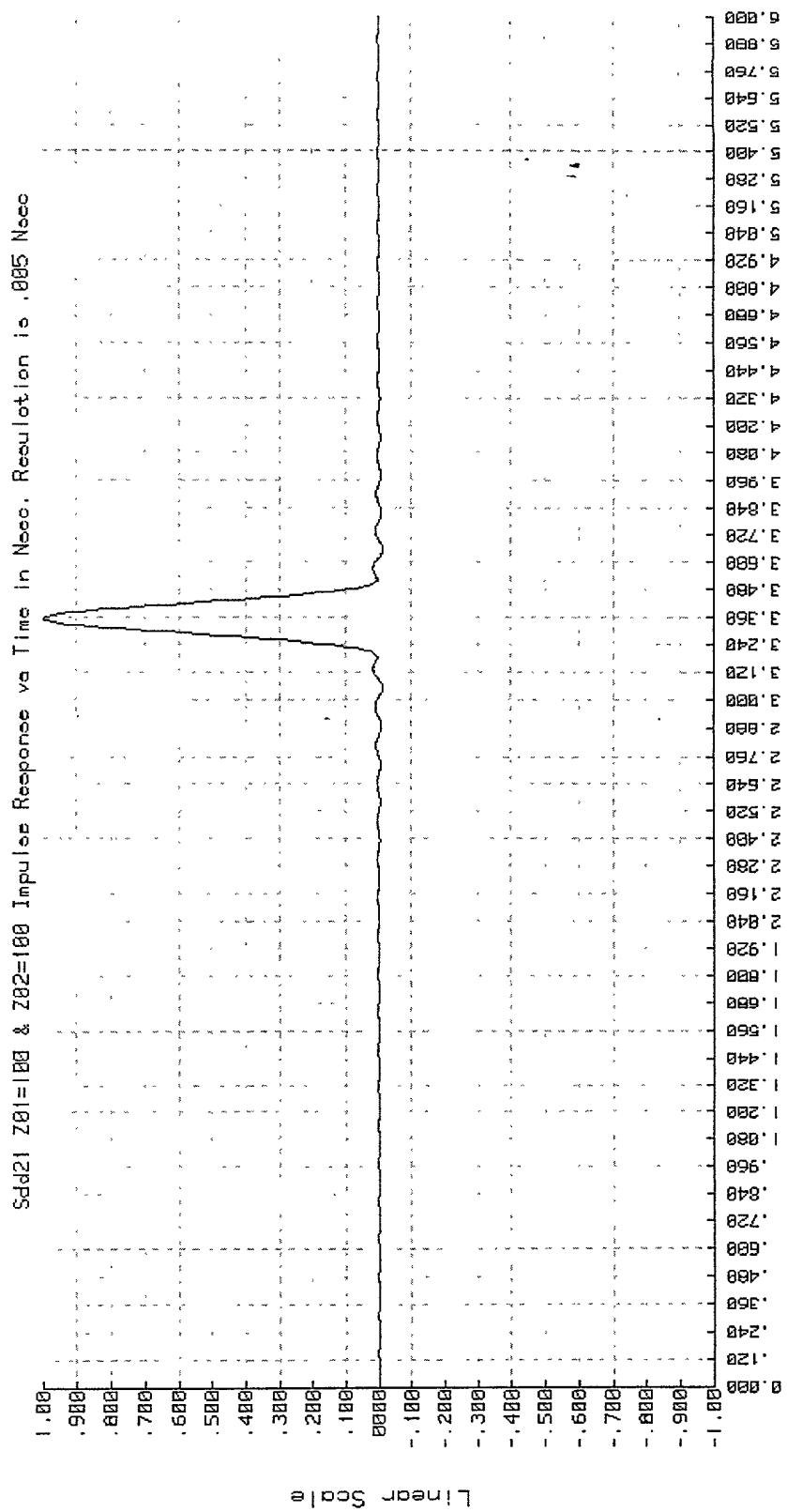


FIGURE 21

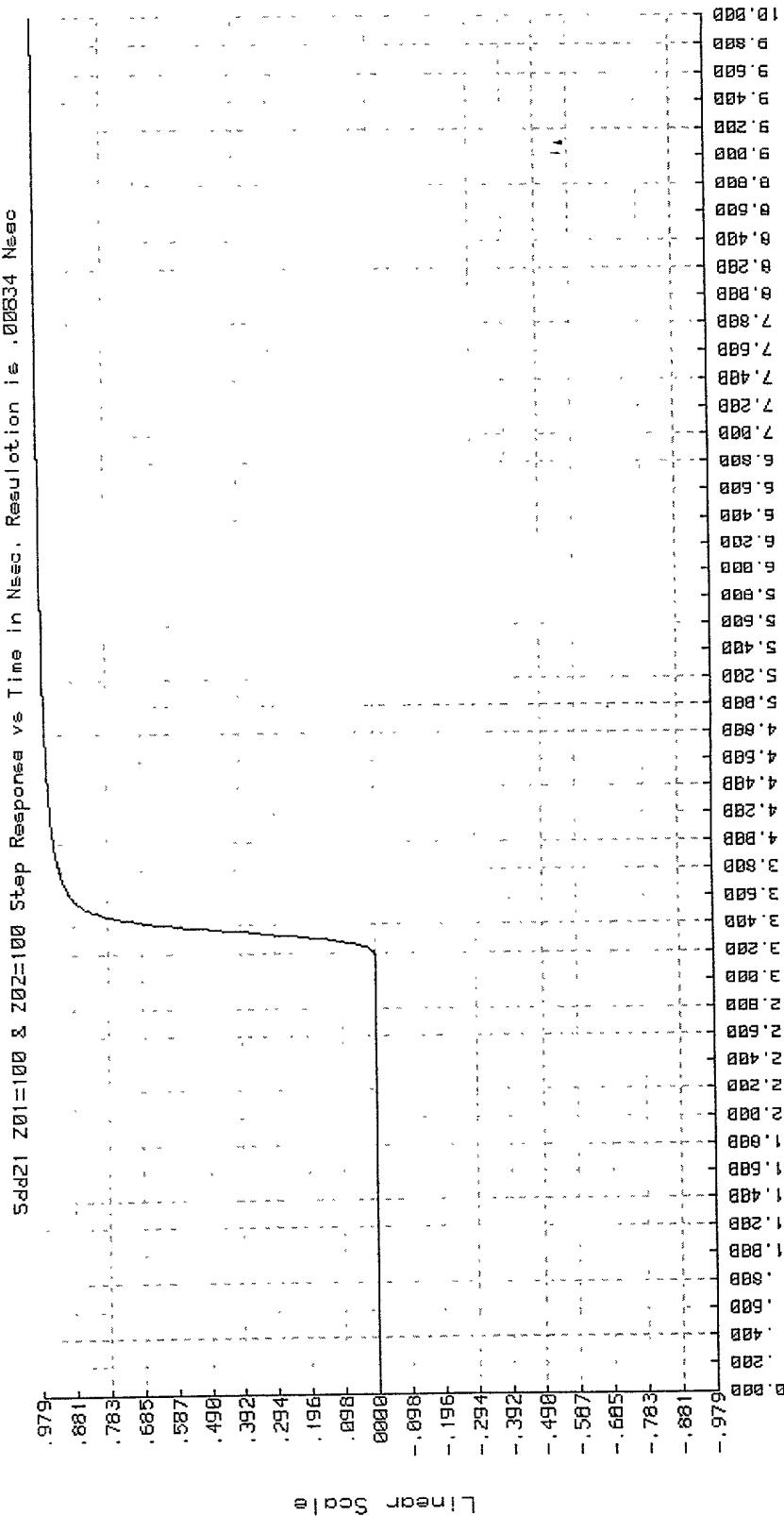


FIGURE 22

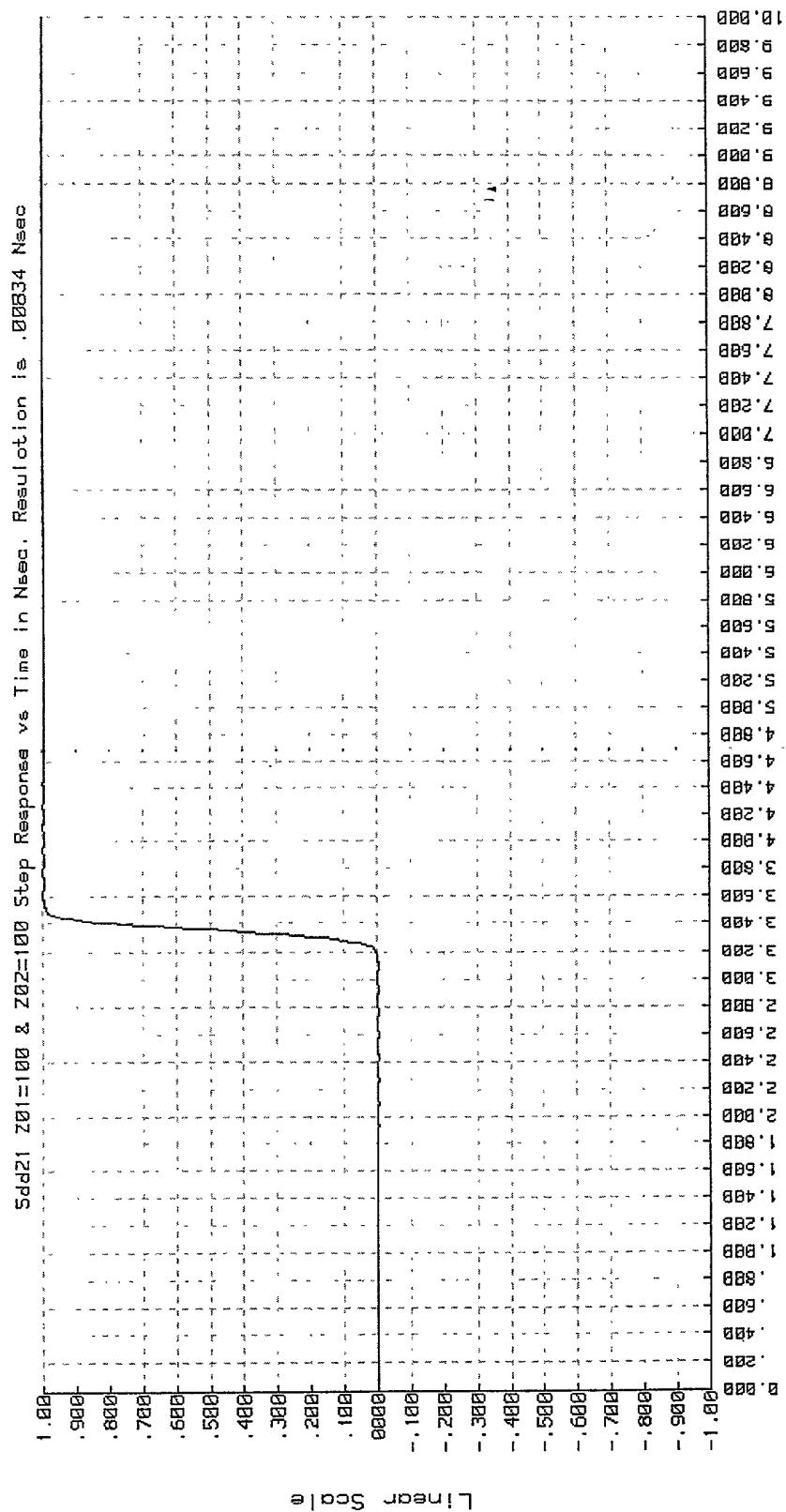


FIGURE 23

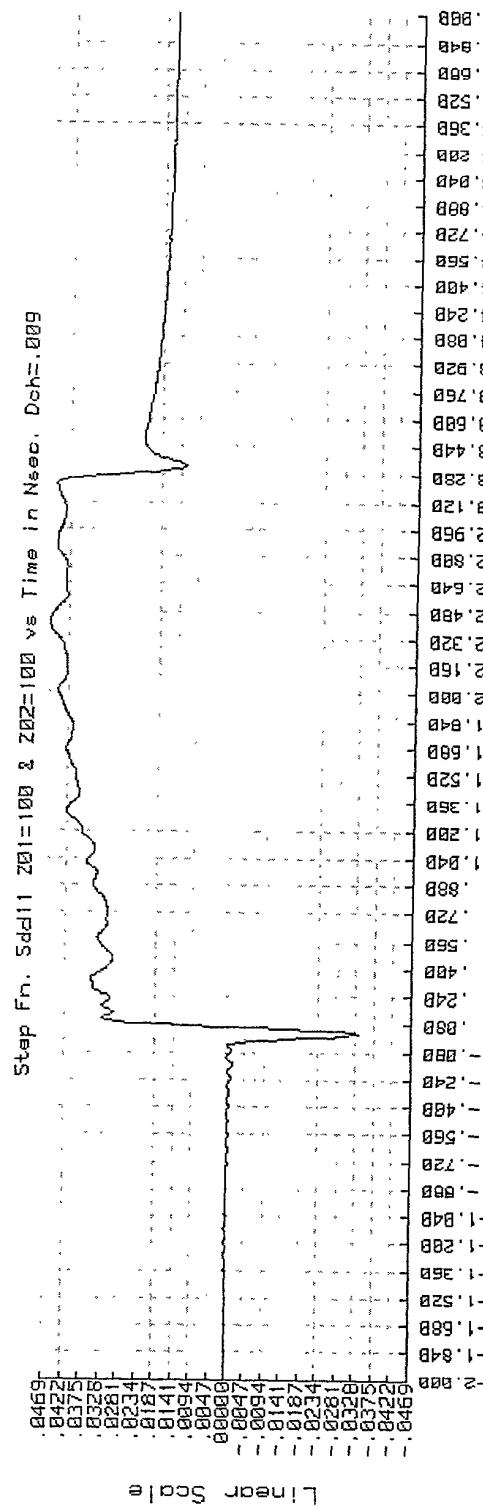


FIGURE 24(a)

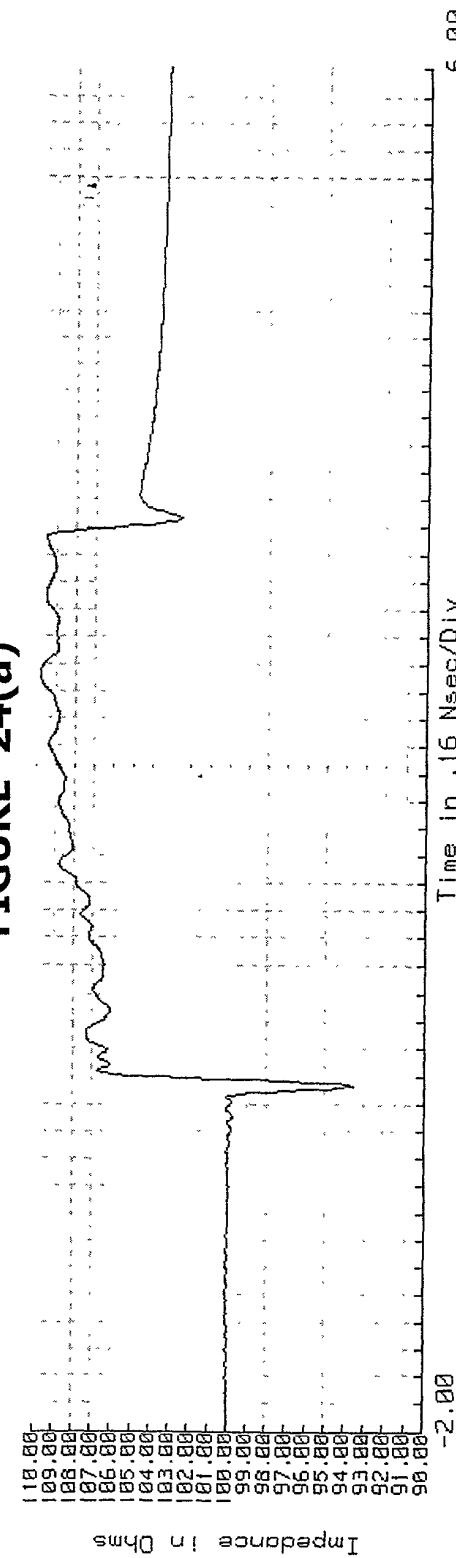


FIGURE 24(b)

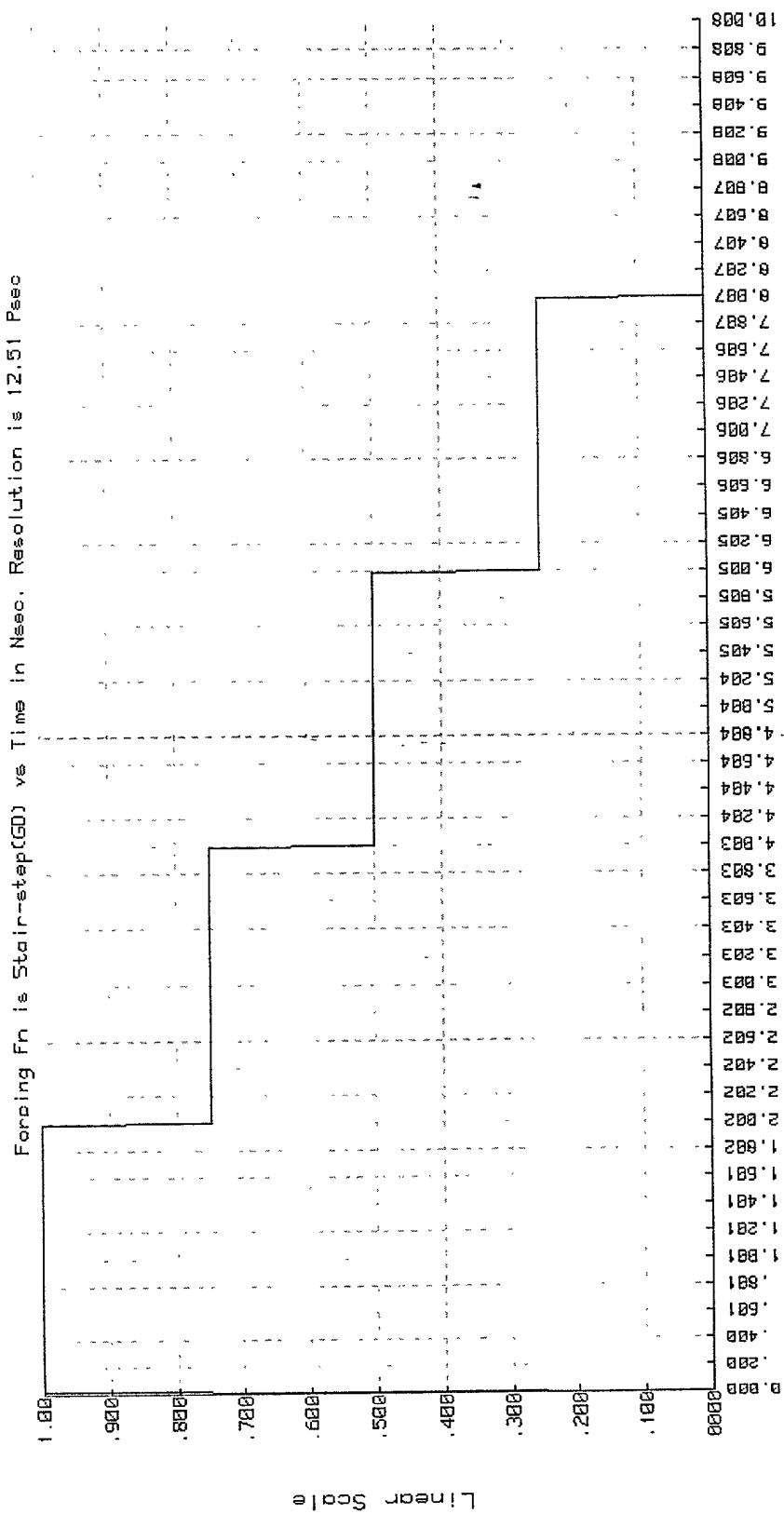


FIGURE 25

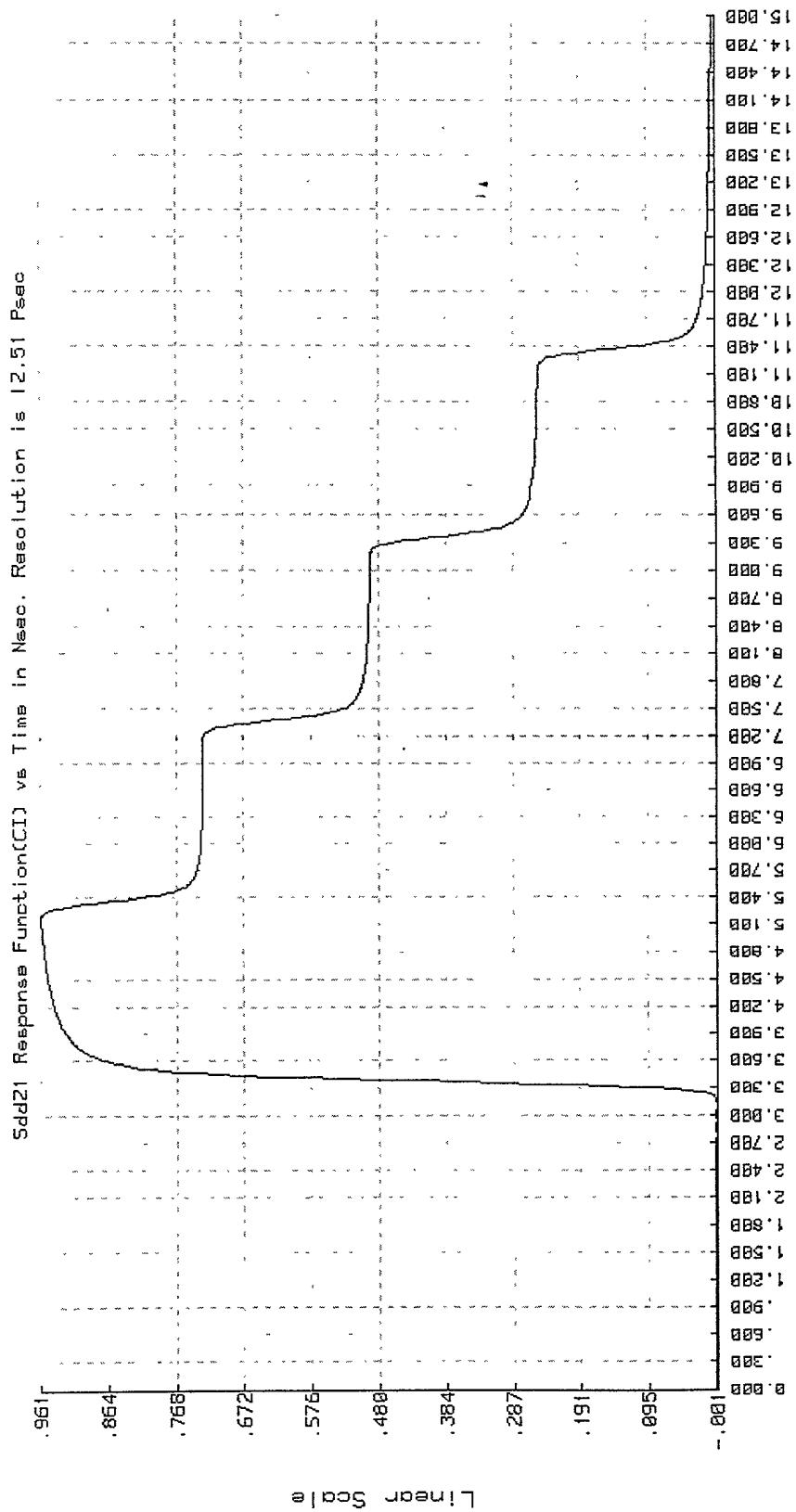


FIGURE 26

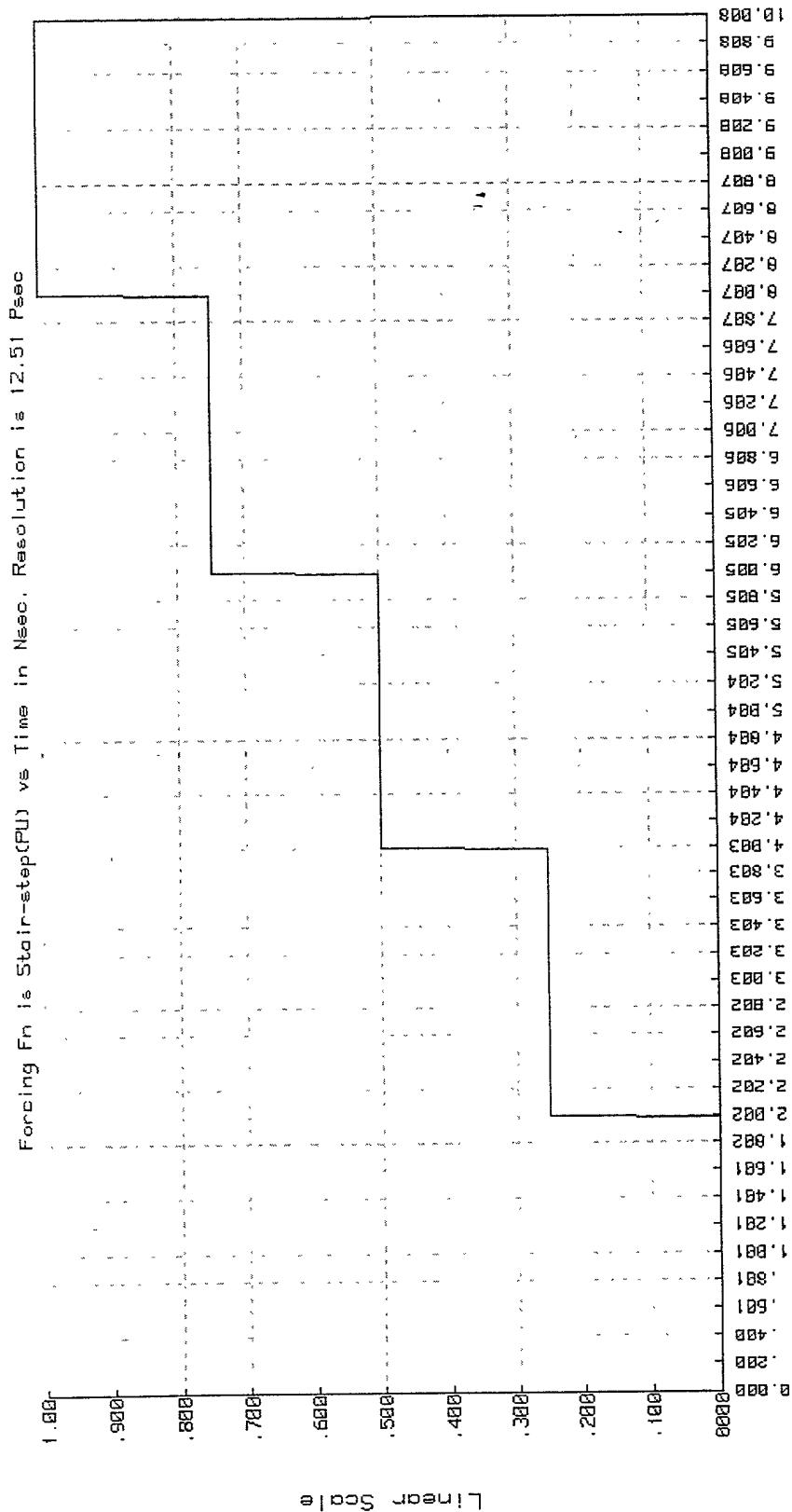


FIGURE 27

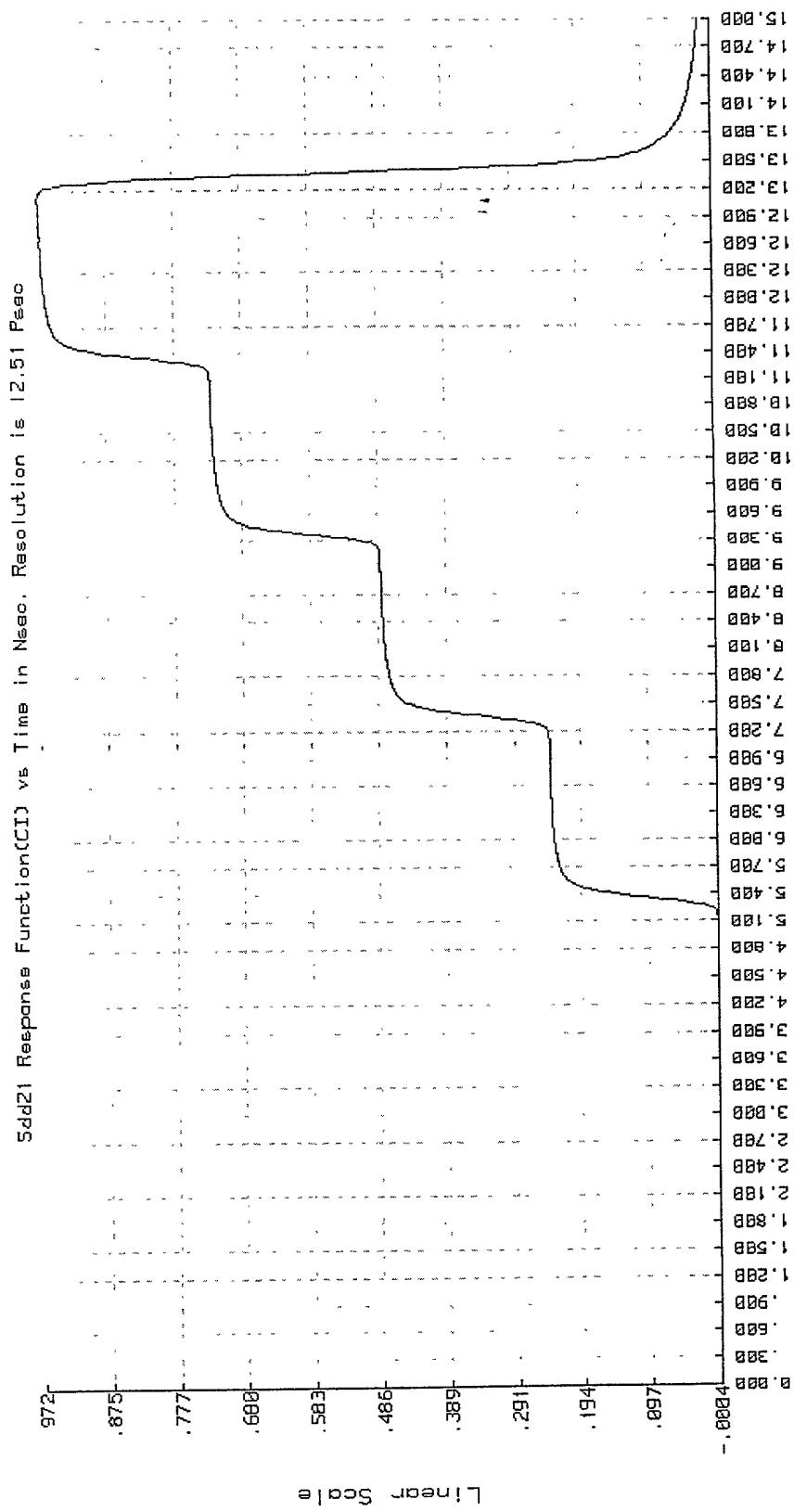


FIGURE 28

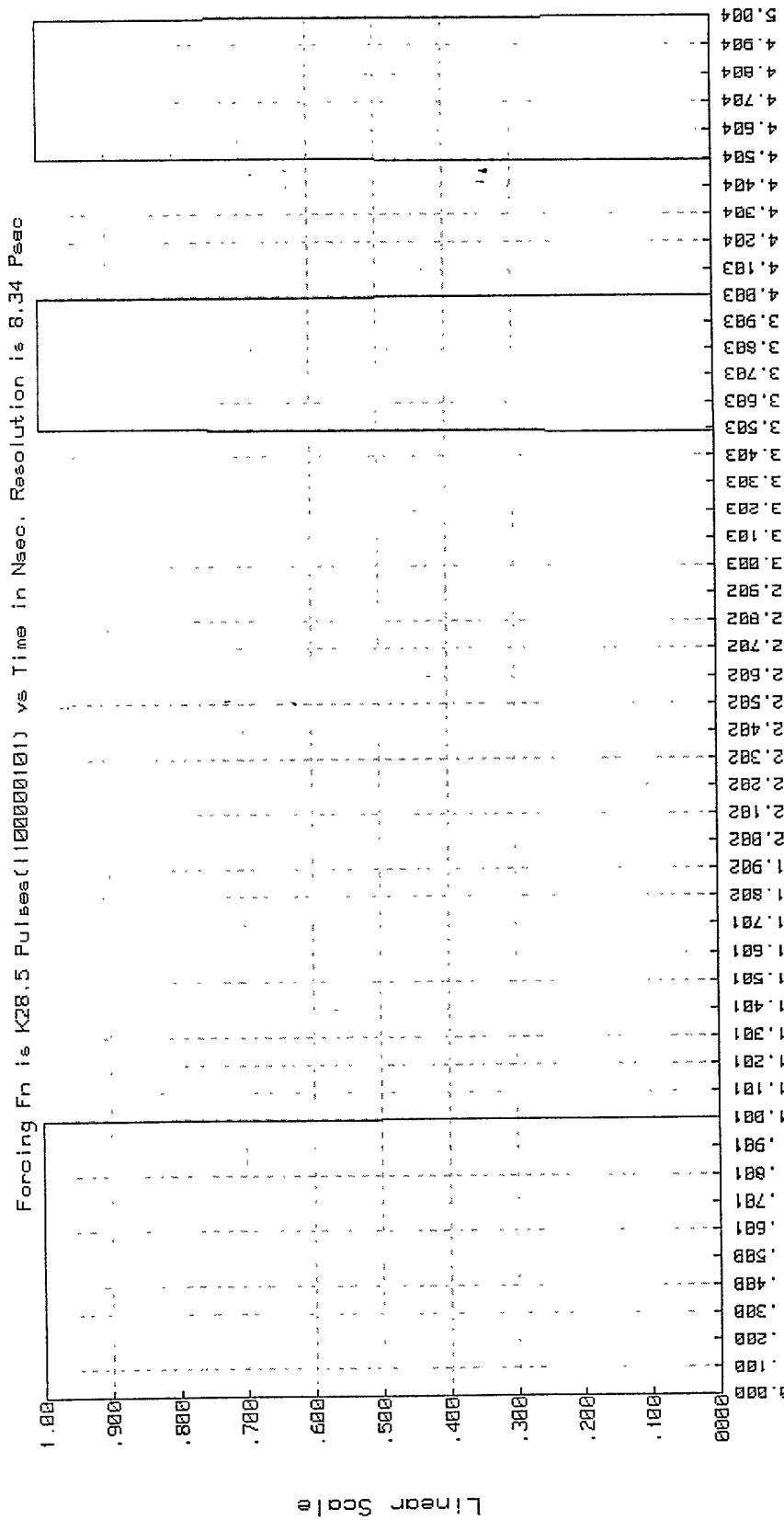


FIGURE 29

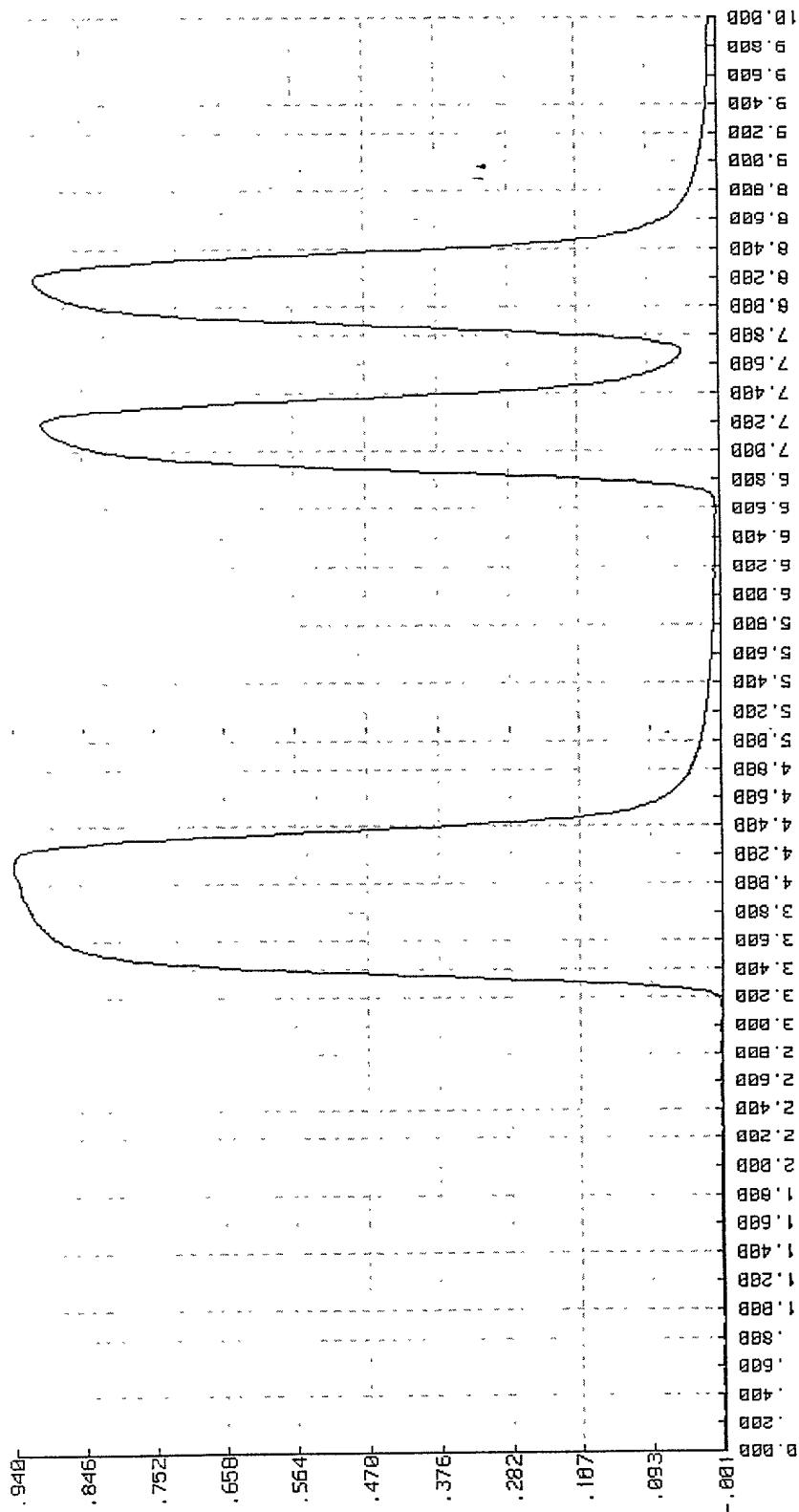


FIGURE 30

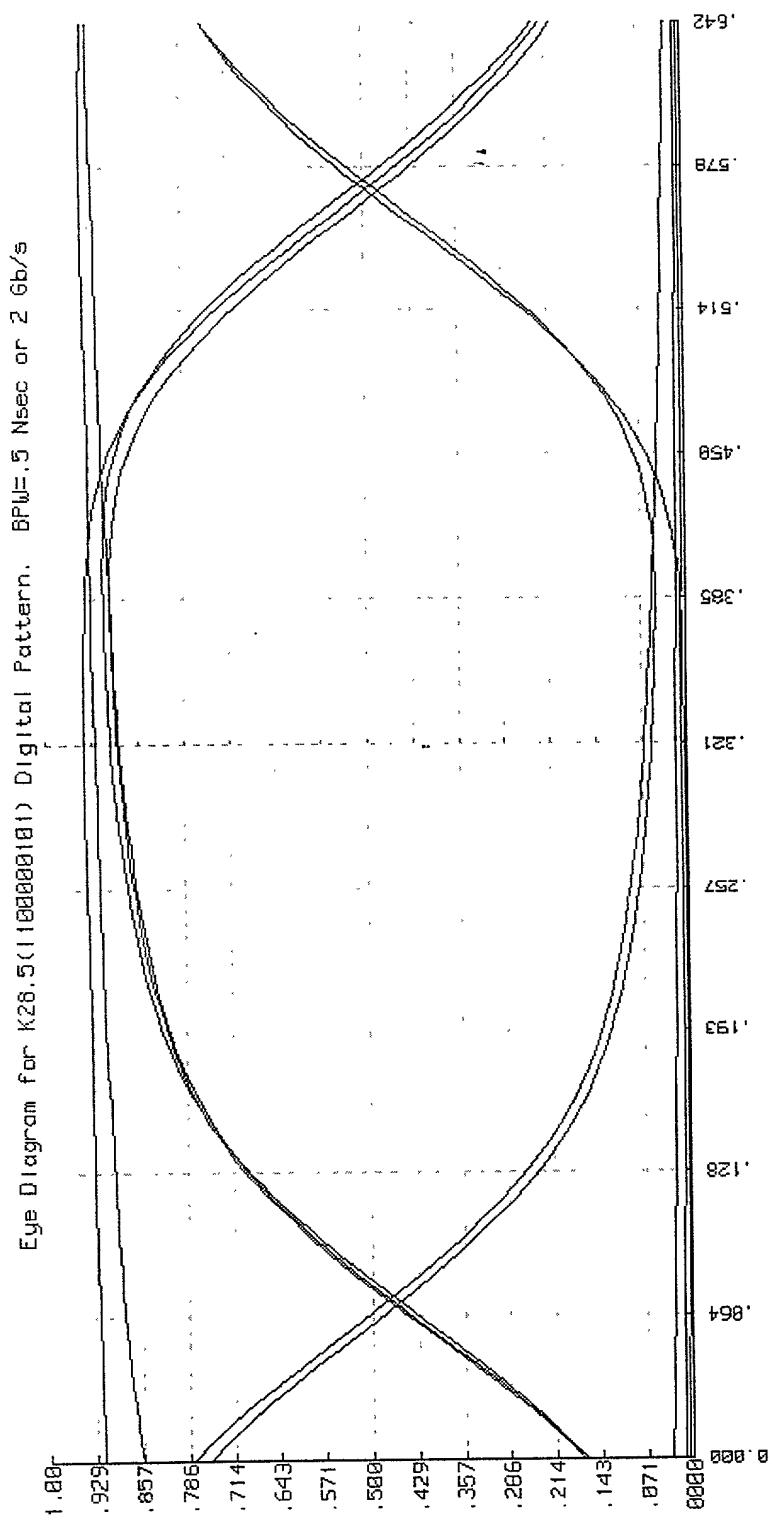


FIGURE 31

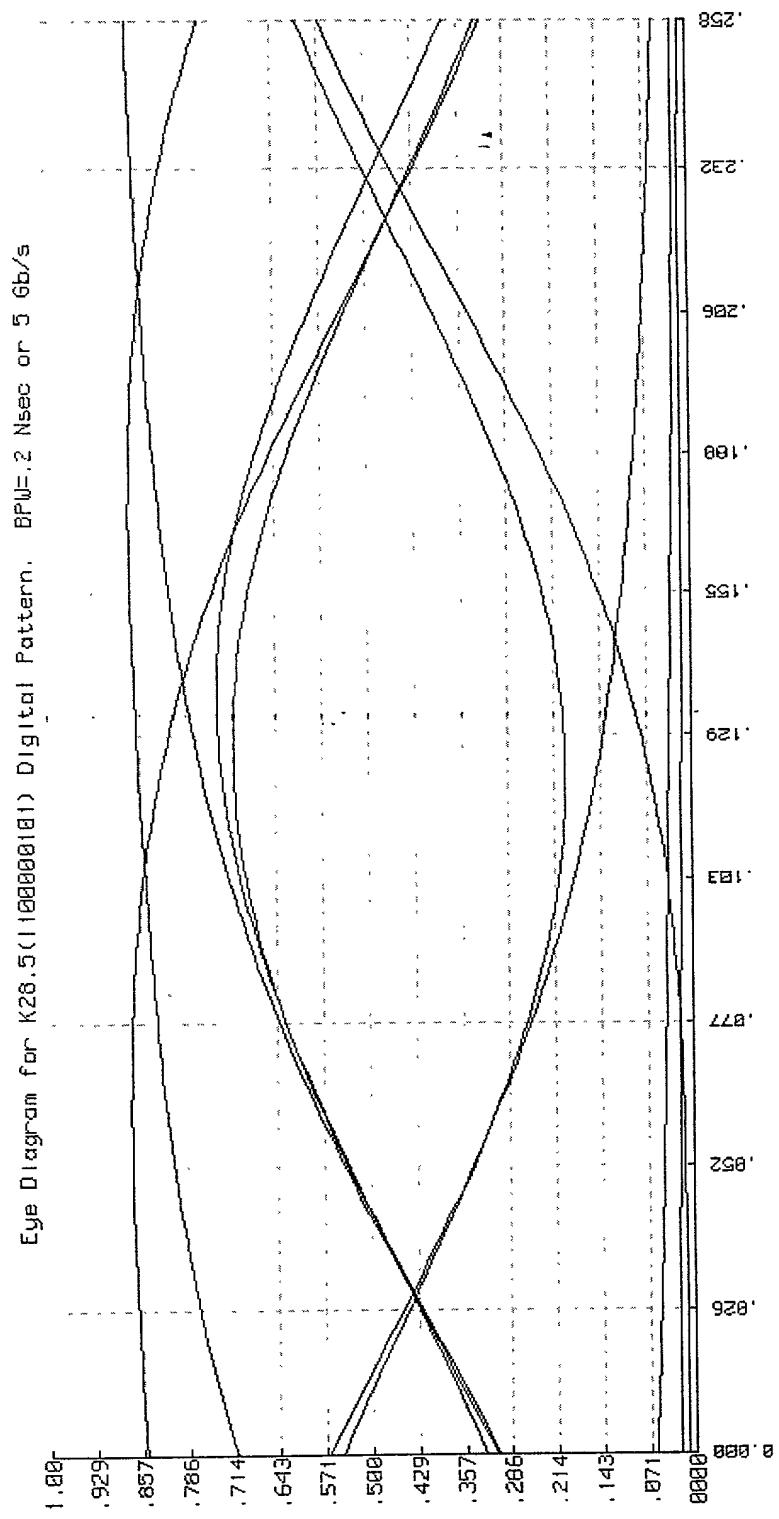


FIGURE 32

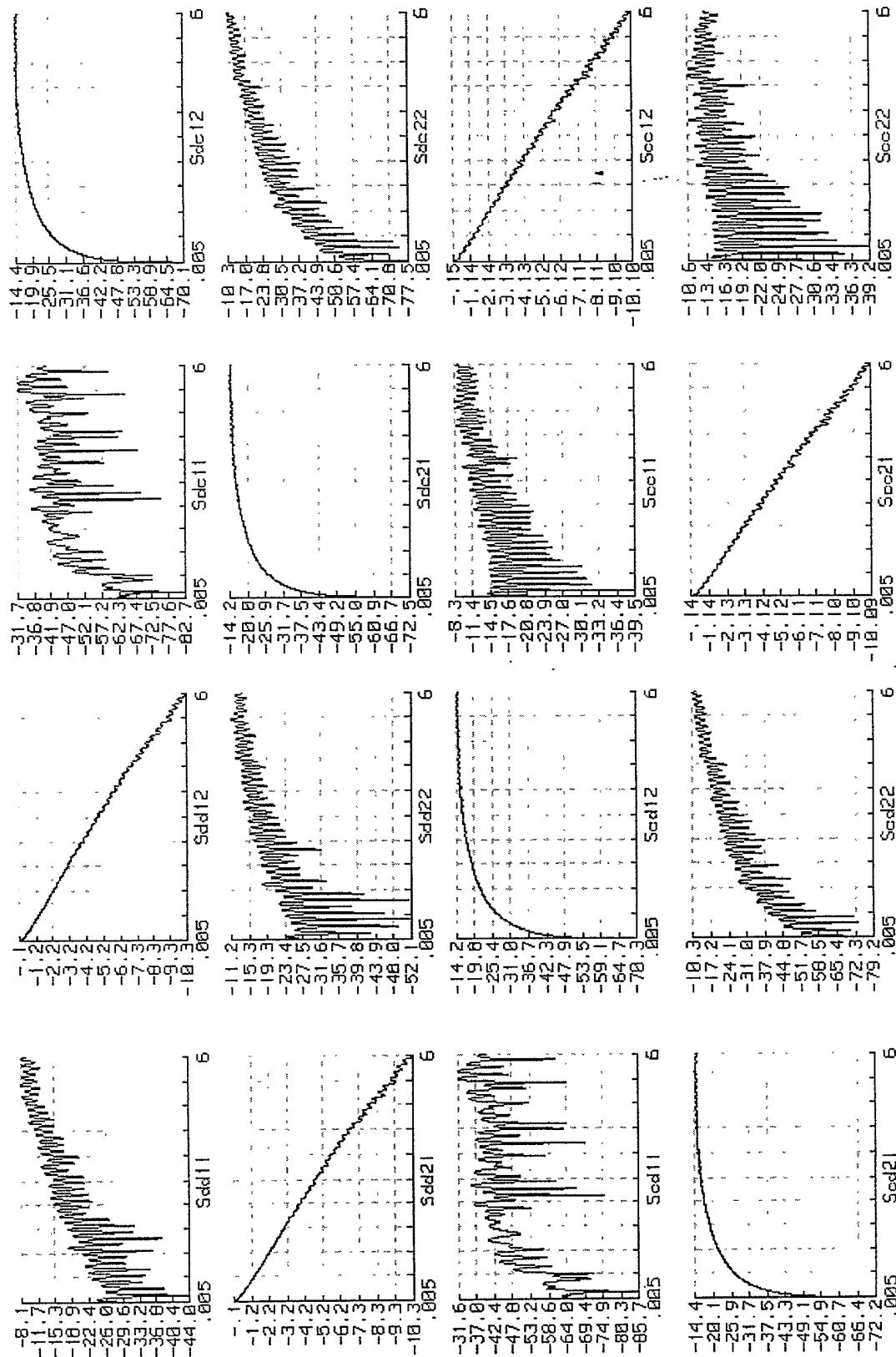


FIGURE 33

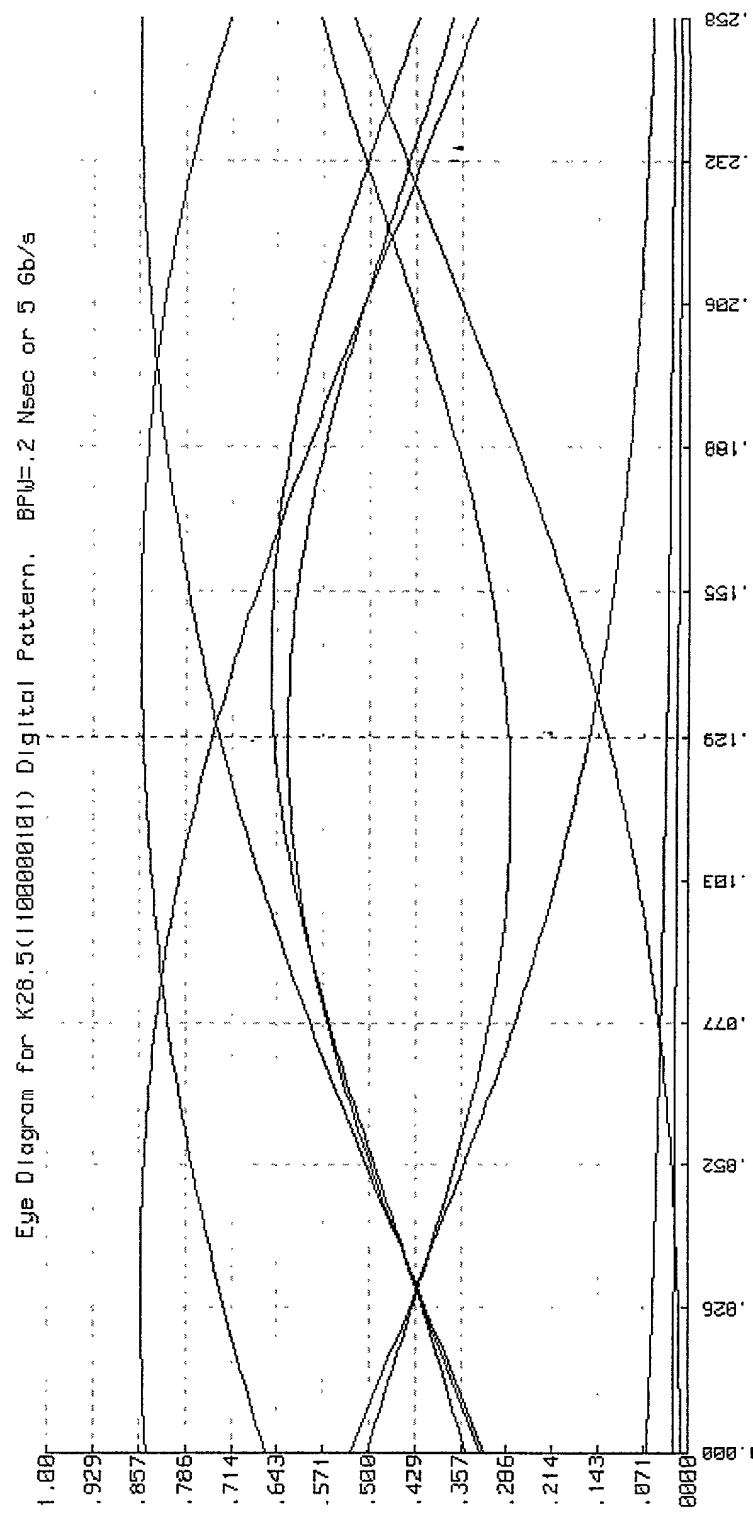


FIGURE 34